What is Claimed is:

1. An address counter strobe test mode device, comprising:

a reference pulse generator means for receiving an external clock signal and generating an internal clock signal;

an address counter strobe test mode means for receiving the internal clock signal and outputting an address strobe signal, wherein a pulse width and a pulse generating time of the address strobe signal are regulated in response to a plurality of received control signals ;

an internal address counter means for receiving an external address signal and outputting an internal address signal in response to the address strobe signal; and

an address decoding means for decoding the internal address signal.

2. The address counter strobe test mode device according to claim 1, further comprising a pad coupled to the internal address counter means and disposed outside so that it is accessible for testing the internal address signal.

3. The device according to claim 1, wherein the address counter strobe test mode means comprises:

a pulse generating time controller means for delaying

the internal clock signal and controlling a pulse generating time in response to a first control signal and a second control signal of the plurality of control signals; and

a pulse width controller means for controlling a pulse width of the internal clock signal in response to a third control signal and a fourth control signal of the plurality of control signals.

4. The device according to claim 3, wherein the pulse generating time controller means comprises:

a decoder means for decoding the first control signal and the second control signal and outputting a plurality of output signals in response thereto;

a plurality of logic operation means for logically operating the internal clock signal and the plurality of output signals from the decoder; and

a plurality of delay unit means for delaying output signals from the logic operation means depending on states of the first control signal and the second control signal.

5. The device according to claim 4, further comprising a plurality of NAND operation means each for performing a NAND operation on output signals from the plurality of delay units, and a NOR gate configured to perform a NOR operation on NAND operation results.

6. The device according to claim 3, wherein the pulse width controller means comprises:

a plurality of transmission gate means for transmitting the internal clock signal in response to the second control signal;

a first logic means for narrowing a pulse width of the internal clock signal; and

a second logic means for widening a pulse width of the internal clock signal.

7. An dynamic random access memory, comprising:

a mode register set configured to generate a plurality of control signals;

a reference pulse generator circuit configured to receive an external clock signal and generate an internal clock signal in response thereto;

an address counter strobe test mode circuit configured to receive the internal clock signal and the plurality of received control signals and output an address strobe signal having a pulse width and a pulse transition time controlled in response to the plurality of received control signals;

an internal address counter circuit configured to receive an external address signal and the address strobe signal and output an internal address signal in response

thereto; and

an address decoding circuit configured to receive and decode the internal address signal.

8. The dynamic random access memory according to claim 7, further comprising a pad coupled to the internal address counter circuit and disposed so that it is accessible for testing the internal address signal.

9. The dynamic random access memory according to claim 7, wherein the address counter strobe test mode circuit comprises:

a pulse generating time controller circuit comprising logic and delay circuits configured to receive the internal clock signal and a first control signal and a second control signal of the plurality of control signals, and generate an intermediate clock signal delayed with respect to the internal clock signal depending on the received first and second control signals; and

a pulse width controller circuit comprising logic and delay circuits configured to receive the intermediate clock signal and a third control signal and a fourth control signal of the plurality of control signals, and generate the address strobe signal having a pulse width determined in response to the third and fourth control signals.

10. The dynamic random access memory according to claim 9, wherein the pulse generating time controller circuit comprises:

a decoder circuit configured to receive the first control signal and the second control signal, and output a plurality of decoder output signals in response thereto;

a plurality of delay circuits each configured to receive the internal clock signal and output an associated clock signal having a predetermined delay, wherein each of the plurality of delay circuits has a different predetermined delay; and

a plurality of logic circuits configured to receive the plurality of decoder output signals and, in response thereto, connect one of the plurality of delay circuits to the internal clock signal to generate the intermediate clock signal.

11. The dynamic random access memory according to claim 10, wherein the plurality of logic circuits comprises:

a plurality of NAND gates each configured to receive two or more of the output clock signals from the plurality of delay circuits and generate a NAND output; and

a NOR gate configured to receive two or more of the plurality of NAND outputs and generate a NOR output; and

an inverter configured to receive the NOR output and

output the intermediate clock signal.

12. The dynamic random access memory according to claim 10, wherein the plurality of logic circuits comprise NAND gates.

13. The dynamic random access memory according to claim 10, wherein the plurality of delay circuits each comprises a number of inverters configured to delay the associated clock signal depending on the number of inverters in the delay circuit.

14. The dynamic random access memory according to claim 13, wherein the plurality of delay circuits comprises four delay circuits that comprise zero, two, four and six inverters respectively.

15. The dynamic random access memory according to claim 9, wherein the pulse width controller circuit comprises:

a plurality of transmission gates configured to receive the intermediate clock signal and the second control signal and transmit the intermediate clock signal in response to the second control signal;

a first logic circuit configured to narrow the pulse width of the internal clock signal; and

a second logic circuit configured to for widen the pulse width of the internal clock signal.

16. The dynamic random access memory according to claim 15, wherein the first logic circuit comprises a NAND gate.

17. The dynamic random access memory according to claim 15, wherein the second logic circuit comprises a NOR gate.

18. A dynamic random access memory, comprising:

a means for receiving an external clock signal having a frequency; and

a means for generating an address strobe signal having a pulse width and delay with respect to the external clock signal that is controlled to prevent mis-operations caused by mis-addressing as the clock signal frequency is increased.